Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of providing a signaling pattern for a bus having a plurality of bit lines, said method comprising:

for each selected bit line in said plurality of bit lines, a memory controller:

selecting a first group of at least one of a plurality of signals comprising a set of pseudo-randomly generated bits to be sent over said selected bit line;

further selecting a second group of at least one of said plurality of signals to be sent over at least one bit line in said plurality of bit lines other than said selected bit line;

transmitting said first group of signals on said selected bit line; and

transmitting said second group of signals over said at least one bit line in said plurality of bit lines other than said selected bit line.

2. (Original) The method of claim 1, wherein said selecting is performed simultaneously with said further selecting.

3. (Cancelled)

4. (Original) The method of claim 1, wherein each signal sent over said selected bit line is identical to each corresponding signal sent over said at least one bit line in said plurality of bit lines other than said selected bit line.

5. (Original) The method of claim 1, wherein the number of bit lines in said plurality of bit lines is 2^N, where $N \geq 1$.

6. (Original) The method of claim 1, further comprising:

storing said plurality of signals in a serial presence detect circuit;

transferring said plurality of signals stored in said serial presence detect circuit into a memory controller; and

performing said selecting and further selecting from said plurality of signals transferred into said memory controller.

7. (Currently Amended) A method of signaling a bus having a plurality of bit lines, said method comprising:

transmitting one of a plurality of signals comprised of a set of pseudo-randomly generated bits on a selected one of said plurality of bit lines;

simultaneously transmitting one of said plurality of signals on one or more of said plurality of bit lines other than said selected bit line; and

repeating said transmitting and simultaneously transmitting for each bit line in said plurality of bit lines, wherein said transmitting, simultaneously transmitting, and repeating are performed using a memory controller.

8. (Cancelled)

9. (previously presented) The method of claim 7, wherein each signal sent over said selected bit line is identical to each corresponding signal sent over said one or more of said plurality of bit lines other than said selected bit line.

10. (previously presented) A method of operating a processor connected to a memory through a bus, said method comprising:

transmitting one of a plurality of signals comprised of a set of pseudo-randomly generated bits on a selected one of a plurality of bit lines in said bus;

simultaneously transmitting one of said plurality of signals on one or more of said plurality of bit lines other than said selected bit line; and

performing a data write/read operation at a data storage location in said memory using said bus while said signals in said transmitting and simultaneously transmitting are present on respective bit lines in said bus.

11. (Original) The method of claim 10, wherein said performing includes:

performing reading of data as part of said data write/read operation in conjunction with a strobe signal received from a delay locked loop.

12. (Original) The method of claim 11, further comprising:

configuring said delay locked loop to provide a delay to said strobe signal so as to enable latching of said data during reading thereof.

13. (Original) The method of claim 12, further comprising determining a duration of said delay based on accuracy of said data read.

14. (Original) The method of claim 13, further comprising repeating said transmitting, simultaneously transmitting, performing and determining for each bit line in said plurality of bit lines.

15. (Original) The method of claim 10, further comprising:

changing an operating condition of said memory, wherein said operating condition includes one or more of a supply voltage, a reference voltage, and temperature; and

repeating said transmitting, simultaneously transmitting, and performing with said changed operating condition present.

16. (Original) A system comprising:

a plurality of memory cells to store data;

a serial presence detect circuit containing a plurality of test bits;

a bus having a plurality of bit lines; and

a memory controller in communication with said plurality of memory cells and said serial presence detect circuit via said bus, wherein said memory controller is configured to:

store therein said plurality of test bits received from said serial presence detect circuit via said bus,

transmit a first one of said plurality of test bits on a selected one of said plurality of bit lines in said bus,

also transmit a second one of said plurality of test bits on one or more of said plurality of bit lines other than said selected bit line, and

facilitate a data write/read operation at one of said plurality of memory cells using said bus while said first one and said second one of said plurality of test bits are present on respective bit lines in said bus.

17. (Original) The system of claim 16, wherein said memory controller is configured to transmit said first one of said plurality of test bits instead of said second one of said plurality of test bits on said one or more of said plurality of bit lines other than said selected bit line.

18. (Original) The system of claim 16, wherein said memory controller is configured to transmit said first one and said second one of said plurality of test bits simultaneously.

19. (Original) The system of claim 18, further comprising:

a delay locked loop circuit configured to provide a delayed strobe signal during reading of data as part of said data write/read operation.

20. (Original) A system comprising:

a memory chip having a serial presence detect circuit containing a plurality of test bits and a plurality of memory cells to store data;

a bus having a plurality of bit lines; and

a processor connected to said memory chip via said bus and in communication therewith through said bus, wherein said processor includes:

a memory controller configured to perform the following:

store therein said plurality of test bits received from said serial presence detect circuit via said bus,

transmit a first one of said plurality of test bits on a selected one of said plurality of bit lines in said bus, and

further transmit a second one of said plurality of test bits on one or more of said plurality of bit lines other than said selected bit line.

21. (Original) The system of claim 20, wherein said memory chip further includes:

a plurality of memory cells to store data, wherein each of said plurality of memory cells is in communication with said memory controller, and wherein said memory controller is configured to further perform the following:

enable said processor to perform a data write/read operation at one of said plurality of memory cells using said bus while said first one and said second one of said plurality of test bits are present on respective bit lines in said bus.

22. (Original) The system of claim 21, wherein said processor further includes:

a delay locked loop circuit configured to provide a delayed strobe signal during reading of data as part of said data write/read operation,

wherein said processor is configured to adjust a duration of delay for said delayed strobe signal based on accuracy of said data read during said data write/read operation.

23. (Original) The system of claim 20, wherein the number of bit lines in said plurality of bit lines is 2^N where $N \geq 1$.

24. (Original) The system of claim 20, wherein said memory controller is configured to further perform the following:

transmit each of said plurality of test bits in a sequence on said selected bit line; and

further transmit a shifted version of said sequence on said one or more of said plurality of bit lines other than said selected bit line, wherein the total number of test bits in said shifted version of said sequence is identical to the total number of test bits in said sequence, and wherein said shifted version of said sequence is generated by shifting the position of each test bit in said sequence by a predetermined offset.

25. (Original) The system of claim 24, wherein said predetermined offset ranges in value from one bit to the total number of test bits minus one.